

- (c) Draw the circuit diagram of Astable multivibrator using OPAMP and find the expression for its time period. Show

$$\text{that } f_0 = \frac{1}{2RC} \text{ if } R_1 = 1.16 R_2.$$

5. Attempt any two parts of the following : (2×10=20)

- (a) Define Lock-in-Range, Capture Range and Pull-in-Time as related to PLL. Draw the circuit diagram of Frequency multiplier using PLL and explain its working.
- (b) Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of a monostable multivibrator using 555 and find expression for quasi state period.
- (c) Write short note on analog to digital converter.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2117 Roll No.

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B. Tech.

(SEM. V) THEORY EXAMINATION 2011-12

### INTEGRATED CIRCUITS

Time : 3 Hours

Total Marks : 100

Note :— Attempt all questions. All questions carry equal marks.

Assume missing data suitably if any.

1. Attempt any two parts of the following : (10×2=20)
- (a) (i) What are desirable characteristics of current mirror circuits? Draw the simple BJT current mirror circuit and reduce the expression for current transfer ratio using matched transistors.
- (ii) What are the advantages of Widlar current source? For the circuit shown in figure 1, assuming high  $\beta$  of transistors and  $V_{BE} = 0.7 \text{ V}$  at  $1 \text{ mA}$ . Find the value of  $R$  that will result in  $I_o = 10 \mu\text{A}$ .

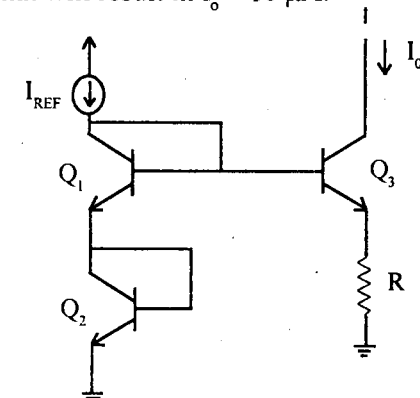


Figure 1

- (b) Explain the role of negative feedback capacitance of  $C_c = 30\text{pF}$  at second stage of OPAMP 741. Find corresponding pole frequency of II<sup>nd</sup> stage gain = 515, output resistance of input stage is  $67\text{M}\Omega$  and input resistance of II<sup>nd</sup> stage is  $4\text{M}\Omega$ .
- (c) Figure 2 shows output stage OPAMP 741. Find output voltage swing. Also explain the role of short circuit protection circuit.

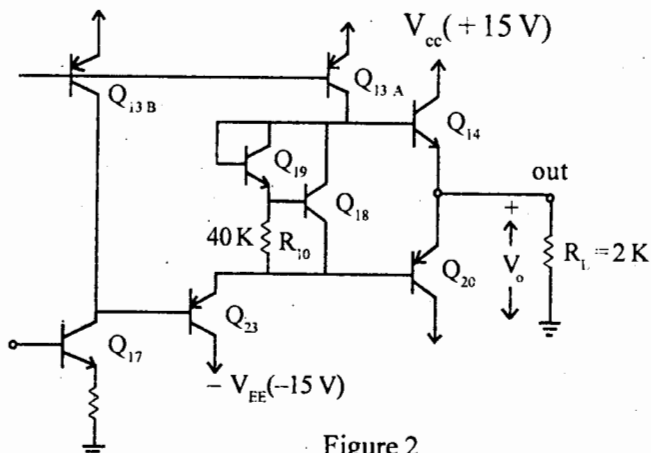
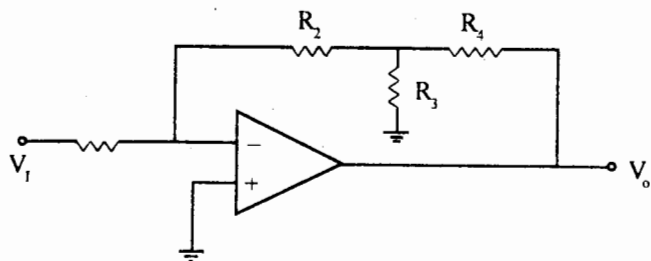


Figure 2

2. Attempt any **two** parts of the following : (10×2=20)

- (a) For the circuit shown in figure 4, find  $\frac{V_o}{V_i}$ .



Design a single stage amplifier to have  $R_i = 1\text{M}\Omega$  and voltage gain hundred.  $N_o$  Resistance should have value greater than  $50\text{M}\Omega$ .

- (b) Draw the circuit diagram of an inductance simulation circuit and find the expression for equivalent inductance.
- (c) Draw the circuit diagram of state variable filter and find the transfer function of Low pass, High pass and Band pass filter.

3. Attempt any **two** parts of the following : (2×10=20)

- (a) Find truth table and CMOS realization of following gates :

(i) AND-OR-INVERT (AOI)  $\Rightarrow F = \overline{AB + CD}$

(ii) OR-AND-INVERT (OAI)  $\Rightarrow F = \overline{(A + B)(C + D)}$

- (b) Give two different CMOS realization of the exclusive-OR function  $Y = A\bar{B} + \bar{A}B$  in which the PDN and PUN are dual networks.

- (c) Give CMOS implementation of a clocked SR flip-flop and explain its working.

4. Answer any **two** parts of the following : (2×10=20)

- (a) Draw the circuit diagram of triangular waveform generator using OPAMP and also find the expression for frequency of the Triangular waveform.

- (b) Draw the circuit diagram of Anti-log amplifier and find the expression for output voltage.